**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1. (original) A trenched DMOS device having a termination structure, the trenched DMOS device comprising:

a silicon substrate of a first conductive type, having a first epitaxial layer of the first conductive type and a second epitaxial layer of a second conductive type formed thereon;

a DMOS trench, formed in the first epitaxial layer and the second epitaxial layer;

a first trench, formed in the first epitaxial layer and the second epitaxial layer disposed close to an edge of the second epitaxial layer, the first trench to be utilized as a main portion of the termination structure having a bottom disposed in the first epitaxial layer;

a second trench disposed between the DMOS trench and the first trench, the second trench having another bottom disposed in the second epitaxial layer adjacent to a region of the second conductive type;

a gate oxide layer on the DMOS trench and the first trench, the gate oxide layer having extended portions covering an upper surface of the second epitaxial layer adjacent the DMOS trench and of the second epitaxial layer adjacent the first trench;

a first polysilicon layer, formed in the DMOS trench;

a second polysilicon layer, formed over the gate oxide layer in the first trench, having another extended portion covering the upper surface of the second epitaxial layer adjacent the first trench, the second polysilicon layer having an opening to expose the gate oxide layer disposed at the bottom of the first trench to split the second polysilicon layer into two discrete parts;

an isolation layer, formed on the first polysilicon layer in the DMOS trench and extended portions of the gate oxide layer adjacent the DMOS trench, on the second polysilicon layer, and on the gate oxide layer over the second epitaxial layer at the bottom of the first trench,

the isolation layer having a first contact window to expose the second polysilicon layer over the second epitaxial layer and a second contact window to expose the second trench; and

a source metal contact layer, formed over the isolation layer and filling both the first contact window and the second contact window, having a connection with a source of the DMOS device and further having an edge beside the first contact window.

2. (original) The trenched DMOS device of claim 1, wherein the isolation layer includes a plurality of body contact windows extending into the second epitaxial layer, and wherein the source metal contact layer is formed over the body contact windows.

3. (original) The trenched DMOS device of claim 1, further comprising a drain metal contact layer formed on a backside surface of the silicon substrate.

4. (original) The trenched DMOS device of claim 1, wherein the isolation layer comprises doped silicate glass.

5. (original) The trenched DMOS device of claim 1, wherein the source metal contact layer comprises a stack of Ti, TiN, and AlSiCu alloy.

6. (original) The trenched DMOS device of claim 1, wherein the first conductive type is an N type and the second conductive type is a P type.

7. (original) The trenched DMOS device of claim 1, wherein the first conductive type is a P type and the second conductive type is an N type.

8. (original) A trenched DMOS device having a termination structure, the trenched DMOS device comprising:

a silicon substrate of a first conductive type, having a first epitaxial layer of the first conductive type and a second epitaxial layer of a second conductive type formed thereon;

a pair of DMOS gates, formed in the first epitaxial layer and the second epitaxial layer and being spaced by a body contact window;

a first trench, formed in the first epitaxial layer and the second epitaxial layer disposed close to an edge of the second epitaxial layer, the first trench to be utilized as a main portion of the termination structure having a bottom disposed in the first epitaxial layer;

a second trench disposed between the DMOS gates and the first trench, the second trench having a bottom disposed in the second epitaxial layer adjacent to a region of the second conductive type;

a gate oxide layer on the first trench, the gate oxide layer having extended portions covering an upper surface of the second epitaxial layer adjacent the first trench;

a second polysilicon layer, formed over the gate oxide layer in the first trench, having another extended portion covering the upper surface of the second epitaxial layer adjacent the first trench, the second polysilicon layer having an opening to expose the gate oxide layer disposed at the bottom of the first trench to split the second polysilicon layer into two discrete parts;

an isolation layer, formed on the DMOS gate, on the second polysilicon layer, and on the gate oxide layer over the second epitaxial layer at the bottom of the first trench, the isolation layer having a first contact window to expose the second polysilicon layer over the second epitaxial layer and a second contact window to expose the second trench; and

a source metal contact layer, formed over the isolation layer and filling both the first contact window and the second contact window, having a connection with a source of the DMOS device and further having an edge beside the first contact window.

9. (original) The trenched DMOS of claim 8 wherein the pair of gates are spaced by a bipolar transistor structure.

10. (original) The trenched DMOS of claim 8 wherein the source metal contact layer is formed over the body contact windows.

11.-22. (canceled)

23. (currently amended) ~~The semiconductor device set of claim 22,~~ A semiconductor device set comprising at least one trench-typed MOSFET and a trench-typed termination structure; wherein the trench-typed MOSFET has a trench profile and comprises a gate oxide layer in the trench profile, and a polysilicon layer on the gate oxide layer; wherein the trench-typed termination structure has a trench profile and comprises an oxide layer in the trench profile, a termination polysilicon layer with discrete features separating the termination polysilicon layer, an isolation layer covering the termination polysilicon layer and filling the discrete features, wherein the at least one trench-typed MOSFET and the trench-typed termination structure are formed on a DMOS device comprising an N+ silicon substrate, an N epitaxial layer on the N+ silicon substrate, and a P epitaxial layer on the N epitaxial layer.

24. (original) The semiconductor device set of claim 23, wherein the trench profiles of the trench-typed MOSFET and of the trench-typed termination structure penetrate through the P epitaxial layer into the N epitaxial layer.

25. (original) The semiconductor device set of claim 23, wherein the DMOS device further comprises a first P region located between the trench-typed termination structure and the trench-typed MOSFET which is adjacent to the trench-typed termination structure, at least one second P region located between the trench-typed MOSFETs, at least one N source region surrounding the trench profiles.